Implementation of Fir Filter using Dadda And Bec Based Addition

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ABSTRACT

Digital filters are widely used in signal processing and communication systems Today most of the processor requires very high speed of operation. Usually DSP processors are based on mathematical approaches. The key blocks of the filter are multipliers and adders, in which multiplier is the one which occupies the major silicon area and consumes more power. In general, the multiplication operations are performed by the shift and add logic. Most of the DSP applications demand faster adders and multipliers for its arithmetic computations. In this project, we propose an area and power efficient FIR filter implementation using Dadda multiplier and binary to excess one converter(BEC) based adder for final merging stages .our proposed system has been coded in Verilog HDL and simulated using Xilinx ,performance analyzed in comparison with booth encoded multiplier

FIR FILTER

In signal processingFinite Impulse Response (FIR) filter is a filter whose impulse response is of finite duration, because it settles to zero in finite time. This is in contrast to infinite impulse response (IIR) filters, which may have internal feedback and may continue to respond indefinitely. The impulse response of an Nth-order discrete-time FIR filter lasts exactly N + 1 samples before it then settles to zero. FIR filters can be discrete-time or continuous-time, and digital or analog. For a causal discrete-time FIR filter of order *N*, each value of the output sequence is a weighted sum of the most recent input values:

$$y[n] = \sum_{k=0}^{N-1} h[k] \cdot x[n-k]$$

where:

- x[n] is the input signal,
- y[n] is the output signal.

An FIR filter has a number of useful properties which sometimes make it preferable to an infinite impulse response (IIR) filter. FIR filters:

- Require no feedback. This means that any rounding errors are not compounded by summed iterations. The same relative error occurs in each calculation. This also makes implementation simpler.
- Are inherently stable, since the output is a sum of a finite number of finite multiples of the input values, so can be no greater than times the largest value appearing in the input.

LITERATURE SURVEY

REVIEW OF LITERATURES

Jer Min Jou, ShiannRongKuang, and Ren Der Chendescribe that, two designs of low-error fixed-width sign magnitude parallel multipliers and two's-complement parallel multipliers for digital signal processing applications are presented. Given two n-bit inputs, the fixed-width multipliers generate n-bit (instead of 2n-bit) products with low product error, but use only about half the area and less delay when compared with a standard parallel multiplier. In them, cost-effective carry-generating circuits are designed, respectively, to make the products generated more accurately and quickly Due to these properties, they are very suitable for use in many multimedia and digital signal processing applications such as digital filtering, arithmetic coding, wavelet transformation, echo cancellation, etc.

Michael J. Schulte and Earl E. Swartzlander,presented a technique for parallel multiplication which computes the product of two numbers by summing only the most significant columns of the multiplication matrix, along with a

correction constant. A method for selecting the value of the correction constant which minimizes the average and mean square error is introduced product. With this technique, the hardware requirements of the multiplier can be reduced by 25 to 35 percent, while limiting the maximum error of the rounded product to less than one unit in the last place.

Yuan-Hao Huang, et al proposes a sub word-detection processing (SDP) technique and a fine-grain soft-error-tolerance (FGSET) architecture to improve the performance of the digital signal processing circuit. In the SDP technique, the logic masking property of the soft error in the combinational circuit is utilized to mask the single-event upset (SEU) caused by disturbing particles in the inactive area. To further improve the performance, the masked portion of the data path can be used as the estimation redundancy in the algorithmic soft error- tolerance (ASET) technique. This technique is called sub word- detection and redundant processing (SDRP). In the FGSET architecture, the soft error in each processing element (fine grain) can be recovered by the arithmetic data path-level ASET technique. Analysis of the fast Fourier transform processor example shows that the proposed FGSET architecture can improve the performance of the coarse-grain SET (CGSET) by 8.5 dB. The low-cost SDP technique (1.03) yields a noise reduction of 5.3 dB over the CGSET approach (1.40), while the efficient SDRP I (1.57) and SDRP II (1.88) techniques outperform the CGSET approach by 24.5 and 30.5 dB, respectively.

DESIGN OF FIR FILTER USING BOOTH RECODED MULTIPLIER

The radix-2 Baugh-Wooley multipliers are rather slow but fast multiplier that uses Booth recoding. A BR4 multiplier, has been considered, where the PPR is fed with less than half of the partial products of those in the BW2 multiplier, thereby providing a much shorter critical path. As opposed to the symmetric BW2 multiplier, in the BR4 topology, the two input operands are processed differently, since *x* is passed to the recoding logic that decides which multiples of *y* should be fed to the PPR. For the considered implementation, a carry-save adder with (m,2) compressors is used for the PPR and a carry-propagate adder is used for the VMA, as in the BW2 multiplier

BINARY EXCESS CODE (BEC)

Carry Select Adder uses single Ripple Carry Adder (RCA) for Cin = 0 Binary Excess Code (BEC) for Cin =1. Using BEC with CSA is to obtain a reduced area and power consumption.Binary to Excess-1 converter is usd to add 1 to the input numbers. One of the RCA is replced with BEC because it requires less number of logic gates for its implementation so the area of the circuit is less.

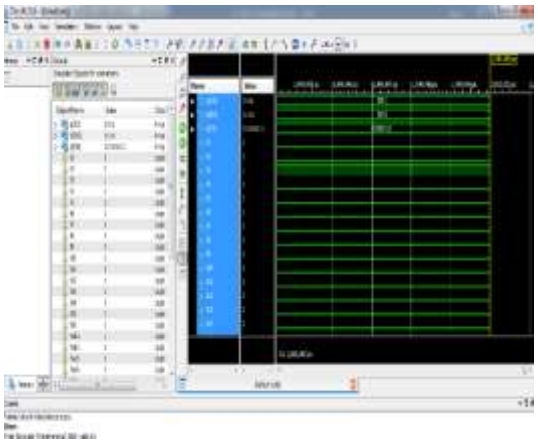
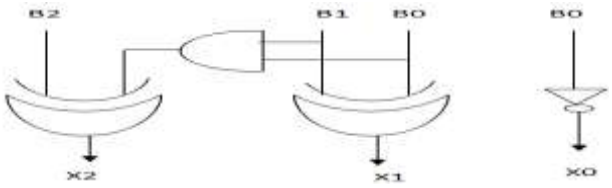


Figure BEC-1 Logic Diagram

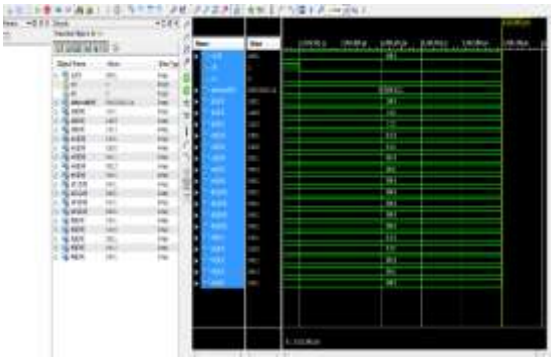
Dadda multipliers are a refinement of the parallel multipliers presented by Wallace. Dadda multiplier consists of three stages. The partial product matrix is formed in the first stage by N2 AND stages. In the second stage, the partial product matrix is reduced to a height of two. Dadda replaced Wallace Pseudo adders with parallel (n, m) counters. A Parallel (n, m) counter is a circuit which has n inputs and produce m outputs which provide a binary count of the ONEs present at the inputs. A full adder is an implementation of a (3, 2) counter which takes 3 inputs and produces 2 outputs. Similarly a half adder is an implementation of a (2, 2) counter which takes 2 inputs and produces 2 outputs. In Dadda multipliers that reduce the number of rows as much as possible on each layer, Dadda multipliers do as few reductions as possible. Because of this, Dadda multipliers have less expensive reduction phase, but the numbers may be a few bits longer, thus requiring slightly bigger adders

- **SIMULATION OUTPUT**
- Finally the FIR filter digital architecture was designed and simulate the final architecture. The



binary data inputs are given and corresponding clock signal is applied either 0 or 1. The stimulation result is shown in Fig

Fig Simulation of multiplier



CONCLUSION

Finally, the design of FIR filter using Dadda multiplier was designed. The complexity of the design is reduced. The speed of the processor is increased in this multiplier. The time taken for multiplication operation by FIR filter processor is reduced by employing BEC based addition algorithm. The high-speed multiplication operation plays vital part in Digital Signal Processor (DSPs) as well as in general processor**.** By using our proposed technique can achieve higher performance and quality for the new technology devices. The proposed block diagram in terms of area, time delay and power of FIR filter with Dadda multiplier is reduced.

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